REMARKS

Introduction

Claims 1-12 are pending in this application. Claims 4-5 and 10-12 have been amended. Claims 1-3 and 6-9 have been cancelled, without prejudice. The Amendments made are fully supported by the specification as filed. No new matter has been introduced.

Claims Rejected Under 35 U.S.C § 102

Claims 1 and 6 have been rejected under 35 U.S.C. §102(b) as being anticipated by Klemmer et al., U.S. Patent No. 6,420,917. Applicants have cancelled claims 1 and 6 without prejudice. Hence, the rejection is moot with respect to those claims.

Claims Rejected Under 35 U.S.C § 103

Claims 1-12 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Lin et al., U.S. Patent No. 7,016,450 (hereinafter "Lin") in view of Callahan, U.S. Patent No. 4,344,050.

Applicants have cancelled independent claims 1 and 6, and have amended claims 4 and 10 to incorporate the features of cancelled claims 1 and 6 and to further clarify the intended subject matter of this disclosure. Applicants respectfully submit that the pending claims as amended, are patentable over the prior art for at least the following reasons.

Newly amended independent claim 4 recites a switched capacitor filter for receiving a current signal and outputting a voltage signal, the switched capacitor filter that includes at least a first capacitor provided between an input terminal for the current signal and a reference voltage, a switched capacitor circuit provided between the input terminal and the first capacitor, and a second capacitor provided in parallel to the first capacitor and the switched capacitor circuit. Furthermore, the switched capacitor circuit includes a first terminal provided on a side of the first

capacitor, a second terminal provided on a side of the input terminal, a plurality of at least three capacitors each having one end to which a reference voltage is supplied and substantially the same capacitance, and a switching section for switching a connection state between the other end of each of the plurality of at least three capacitors and an associated one of the first and second terminals. Further, in the switched capacitor circuit, the switching section connects the other end of the other one of the other two to the second terminal, while maintaining connection between the other end of one of the plurality of at least three capacitors and the second terminal, when the switching section connects the other end of one of other two of the plurality of at least three capacitors to the first terminal.

The Examiner admits that Lin does not disclose or suggest the features of claim 1 of "that the resistor (Rp) includes a switch capacitor circuit," but relies on Callahan in an attempt to obviate this deficiency of Lin.

Lin discloses a clock recovery circuit for generating an output signal that is synchronized with an input signal. As shown in Fig. 1 of Lin, a data recovery circuit 10 can generate an output signal OUT that is synchronized with an input signal IN. The data recovery circuit 10 includes a charge pump 20, a filter 24, and a voltage controlled oscillator 26. The filter 24 includes a capacitor C0 in parallel to resistor Rp and capacitor Cp. However, Lin does not disclose a switched capacitor circuit. As a result, Lin does not disclose a switched capacitor circuit that includes a first terminal provided on a side of the first capacitor, a second terminal provided on a side of the input terminal, a plurality of at least three capacitors each having one end to which a reference voltage is supplied and substantially the same capacitance, and a switching section for switching a connection state between the other end of each of the plurality of at least three

capacitors and an associated one of the first and second terminals, as required by amended claim 4.

Callahan discloses a switched capacitor filter designed to utilize two parallel switched capacitor charge pumps. As shown in Figs. 1 and 5 of Callahan, switches 11 and 12 are connected to capacitors 13 and 14. Further, switches 11 and 12 and capacitors 13 and 14 are in parallel to switches 111 and 112 and capacitor 113. While Callahan may disclose three capacitors connected to ground, only two (capacitors 13 and 113) of the three capacitors (capacitors 13, 14, and 113) are positioned between switches 11 and 12 and switches 111 and 112. Therefore, capacitor 14 does not maintain a connection between the capacitor and the second terminal. As a result, Callahan does not disclose a plurality of at least three capacitors each having one end to which a reference voltage is supplied and substantially the same capacitance, wherein the switching section connects the other end of the other one of the other two to the second terminal, while maintaining connection between the other end of one of the plurality of at least three capacitors and the second terminal, when the switching section connects the other end of one of other two of the plurality of at least three capacitors to the first terminal, as required by amended claim 4.

Accordingly, even assuming arguendo that the combination is proper, Lin and Callahan still fail to disclose or suggest a switched capacitor filter as recited by the pending claims including at least one of the switched capacitor circuit includes a plurality of at least three capacitors each having one end to which a reference voltage is supplied and substantially the same capacitance, and in the switched capacitor circuit, the switching section connects the other end of the other one of the other two to the second terminal, while maintaining connection between the other end of one of the plurality of at least three capacitors and the second terminal,

when the switching section connects the other end of one of other two of the plurality of at least three capacitors to the first terminal.

Similarly, independent claim 10 recites a feedback system for feeding back an output clock generated on the basis of an input clock to make the output clock have a predetermined characteristic, the feedback system that includes at least a charge pump circuit for generating a charge current, on the basis of a phase difference between the input clock and a fed-back clock, a loop filter for receiving the charge current as an input, and an output clock generator circuit for generating the output clock, on the basis of an output signal from the loop filter. Furthermore, the loop filter includes a first capacitor provided between an input terminal for the charge current and a reference voltage, a switched capacitor circuit provided between the input terminal and the first capacitor and a second capacitor provided in parallel to the first capacitor and the switched capacitor circuit. Further, the switched capacitor circuit includes a first terminal provided on a side of the first capacitor, a second terminal provided on a side of the input terminal, a plurality of at least three capacitors each having one end to which a reference voltage is supplied and substantially the same capacitance, and a switching section for switching a connection state between the other end of each of the plurality of at least three capacitors and an associated one of the first and second terminals. Further, in the switched capacitor circuit, the switching section connects the other end of the other one of the other two to the second terminal, while maintaining connection between the other end of one of the plurality of at least three capacitors and the second terminal, when the switching section connects the other end of one of the other two of the plurality of at least three capacitors to the first terminal.

Accordingly, as each and every element of the claims must be disclosed or suggested by the cited prior art references to establish a prima facie case of obviousness (see MPEP §2143),

and for at least the foregoing reasons the combination of Lin and Callahan fails to do so, it is respectfully submitted that claims 4 and 10, as amended, are patentable over the cited prior art.

Under Federal Circuit guidelines, a dependent claim is non-obvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as independent claims 4 and 10 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon (claims 5 and 11-12) are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Conclusion

The Applicants have addressed all rejections/objection raised by the Examiner. Accordingly, it is believed that all pending claims are now in condition for allowance. Applicants therefore respectfully request an early and favorable reconsideration and allowance of this application. If there are any outstanding issues which might be resolved by an interview or an Examiner's amendment, the Examiner is invited to call Applicants' representative at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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